

Analysis and hardware implementation of five level cascaded H Bridge inverter

G. Bhavanarayana, Chavvakula Swamy, Ganta Mounika, yedlapalli netaji, Sundru Sri durga

EEE. pragati engineering college Surampalem, India

EEE. pragati engineering college Surampalem, India

EEE. pragati engineering college Surampalem, India

EEE. pragati engineering college Surampalem, India

EEE. pragati engineering college Surampalem, India

Abstract

The cascaded multilevel inverter (CMLI) has gained much attention in recent years due to its advantages in high voltage and high power with low harmonics applications. A standard cascaded multilevel inverter requires n DC sources for $2n+1$ levels at the output, where n is the number of inverter stages. This paper presents a topology to control cascaded multilevel inverter that is implemented with multiple DC sources to get 2^n+1 levels. Without using Pulse Width Modulation (PWM) technique, the firing circuit can be implemented using Microcontroller which greatly reduces the Total Harmonic Distortion (THD) and switching losses. To develop the model of a cascaded hybrid multilevel inverter, a simulation is done based on MATLAB/SIMULINK software and hardware implementation was also done. Their integration makes the design and analysis of a hybrid multilevel inverter more complete and detailed.

I. Introduction

Recent advances in the power-handling capabilities of static switch devices such as IGBTs with voltage rating up to 4.5 kV commercially available, has made the use of the voltage source inverters (VSI) feasible for high-power applications. High power and high-voltage conversion systems have become very important issues for the power electronic industry handling the large ac drive and electrical power applications at both the transmission and distribution levels. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

Switch-mode dc-to-ac inverters used in ac power supplies and ac motor drives where the objective is to produce a sinusoidal ac output whose magnitude and frequency can both be controlled. Practically, we use an inverter in both single-phase and three phase ac

systems. A half-bridge is the simplest topology, which is used to produce a two level square-wave output waveform. A center-tapped voltage source supply is needed in such a topology. It may be possible to use a simple supply with two well-matched capacitors in series to provide the center tap. Today, multilevel inverters are extensively used in high-power applications with medium voltage levels. The field applications include use in laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on.

II. Multi level inverter

The term multilevel starts with the three-level inverter introduced by Nabae. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems.

An inverter is a device that converts dc input power to ac output power at desired output of voltage and frequency.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM).

III. H Bridge Inverter

“H” topology has many redundant combinations of switches’ positions to produce the same voltage levels. As an example, the level “zero” can be generated with switches in position S(1) and S(2), or S(3) and S(4), or S(5) and S(6), and so on.

Another characteristic of “H” converters is that they only produce an odd number of levels, which ensures the existence of the “0V” level at the load. For example, a 51-level inverter using an “H” configuration with transistor-clamped topology requires 52 transistors, but only 25 power supplies instead of the 50 required when using a single leg. Therefore, the problem related to increasing the number of levels and reducing the size and complexity has been partially solved, since power supplies have been reduced to 50%.

The single-phase H – Bridge of cascaded inverter. The ac terminal voltages of each bridge are connected in series. Unlike the diode clamp or flying capacitors inverter, the cascaded inverter does not require any voltage-clamping diodes or voltage balancing capacitors.

This configuration is useful for constant frequency applications such as active front-end rectifiers, active power filters, and reactive power compensation.

In this case, the power supply could also be voltage regulated dc capacitor. The circuit diagram consists of two cascade bridges. The load is connected in such a way that the sum of output of these bridges will appear across it. The ratio of the power supplies between the auxiliary bridge and the main bridge is 1:3. One important characteristic of multilevel converters using voltage escalation is that electric power distribution and switching frequency present advantages for the implementation of these topologies.

The full-bridge topology is used to synthesize a three-level square-wave output waveform. The half-bridge and full-bridge configurations of the single-phase voltage source inverter are shown in Fig. a and b, respectively. In a single-phase half-bridge inverter, only two switches are needed. To avoid shoot-through fault, both switches are never turned on at the same time. S1 is turned on and S2 is turned off to give a load voltage, V_{AO} in Fig. b, of $+V_s/2$. To complete one cycle, S1 is turned off and S2 is turned on to give a load voltage, V_{AO} , of $-V_s/2$. In full bridge configuration, turning on S1 and S4 and turning off S2 and S3 give a voltage of V_s between point A and B (V_{AB}) in Fig. b, while turning off S1 and S4 and turning on S2 and S3 give a voltage of $-V_s$.

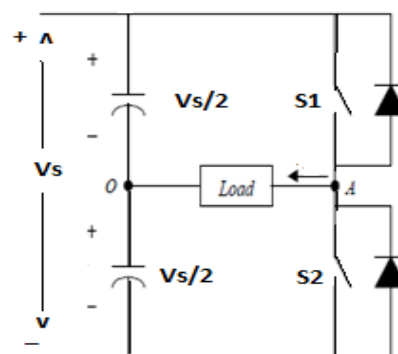


Fig.1. Half Bridge Inverter

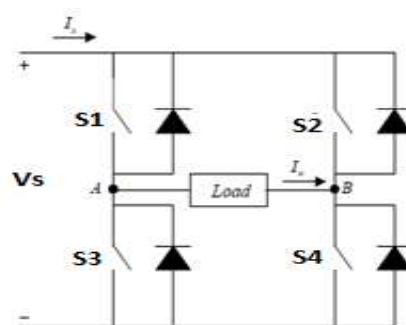


Fig.2. Full Bridge Inverter

To generate zero level in a full-bridge inverter, the combination can be S1 and S2 on while S3 and S4 off or vice versa. The three possible levels referring to above discussion are shown in Table 1

Table 1: Switching pattern of 3 level full bridge inverter

Conducting Switches	Load Voltage V_{AB}
S ₁ ,S ₄	$+V_s$
S ₂ ,S ₃	$-V_s$
S ₁ ,S ₂ or S ₃ ,S ₄	0

Note that S1 and S3 should not be closed at the same time, nor should S2 and S4. Otherwise, a short circuit would exist across the dc source. The output waveform of half bridge and full-bridge of single-phase voltage source inverter are shown in Fig. 2.3 and 2.4 respectively.

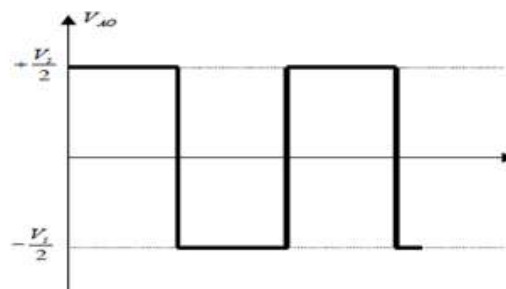


Fig.3. Output waveform of Half Bridge Inverter

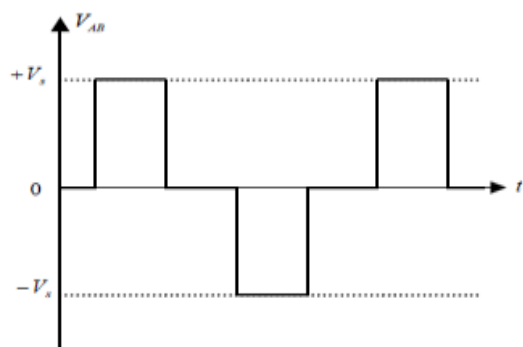


Fig.4. Output waveform of full bridge inverter

IV. Why Cascaded H-bridge multilevel inverter ?

Cascaded H-Bridge (CHB) configuration has recently become very popular in high-power AC supplies. A cascade multilevel inverter consists of a series of H-bridge (single-phase full bridge) inverter units in each of its three phases. The ac terminal voltages of different level inverters are connected in series. Through different combinations of the four switches, S1-S4, each converter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero. The AC outputs of different full-bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. Note that the number of output-phase voltage levels is defined in a different way from those of the two previous converters (i.e. diode clamped and flying capacitor). In this topology, the number of output-phase voltage levels is defined by $m = 2N + 1$, where N is the number of DC sources. A seven-level cascaded converter, for example, consists of three DC sources and three full bridge converters. Minimum harmonic distortion can be obtained by controlling the conducting angles at different converter levels. Each H-bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase legs' switching timings. Each switching device always conducts for 180° (or half cycle) regardless of the pulse width of the quasi-square wave. This switching method makes all of the switching devices current stress equal. In the charging mode, the cascade converters act as rectifiers, and power flows from the charger (ac source) to the batteries. The cascade converters can also act as rectifiers to help recover the kinetic energy of the vehicle if regenerative braking is used. The cascade inverter can also be used in parallel HEV configurations. This new converter can avoid extra clamping diodes or voltage balancing capacitors. The combination of the 180° conducting method and the pattern-swapping scheme make the cascade inverters voltage and current stresses the same and battery voltage balanced. Identical H-bridge inverter

units can be utilized, thus improving modularity and manufacturability and greatly reducing production costs.

V. Multilevel Inverter structures

A voltage level of three is considered to be the smallest number in multilevel converter topologies. Due to the bi-directional switches, the multilevel VSC can work in both rectifier and inverter modes. This is why most of the time it is referred to as a converter instead of an inverter in this dissertation. A multilevel converter can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current. As the number of levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage-imbalance problems, voltage clamping requirements, circuit layout and packaging constraints complexity of the controller, and, of course, capital and maintenance costs.

Three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors. The multilevel inverter structures are the main focus of discussion in this chapter; however, the illustrated structures can be implemented for rectifying operation as well. Although each type of multilevel converters share the advantages of multilevel voltage source inverters, they may be suitable for specific application due to their structures and drawbacks. Operation and structure of some important type of multilevel converters are discussed in the following sections.

In a multilevel VSI, the dc-link voltage V_{dc} is obtained from any equipment which can yield stable dc source. Series connected capacitors constitute energy tank for the inverter providing some nodes to which multilevel inverter can be connected. Primarily, the series connected capacitors will be assumed to be any voltage sources of the same value. Each capacitor voltage V_c is given by $V_c = V_{dc} / (n - 1)$, where n denotes the number of level. Fig. 2.5 shows a schematic diagram of one phase leg of inverters with different number of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor, while the three-level inverter generates three voltages, and so on.

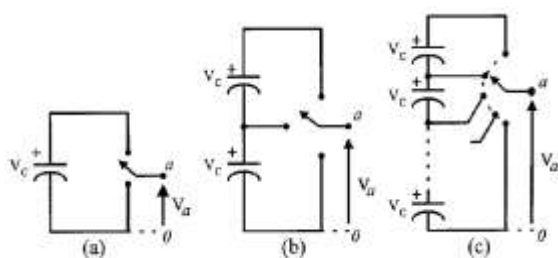


Fig.5. One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels.

Cascaded H-Bridge multilevel Inverter

The cascaded H-bridge multilevel Inverter uses separate dc sources (SDCSs). The multilevel inverter using cascaded-inverter with SDCSs synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from either batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. Again, the cascaded multilevel inverters are classified depending the type of DC sources used throughout the input.

A single-phase structure of an m-level cascaded inverter is Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1 , S_2 , S_3 , and S_4 . To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3 . By turning on S_1 and S_2 or S_3 and S_4 , the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs.

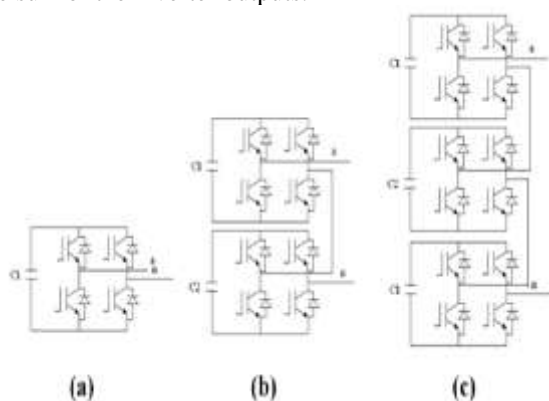


Fig.6. Single phase structures of Cascaded inverter (a) 3-level, (b) 5-level, (c) 7-level

One more alternative for a multilevel inverter is the cascaded multilevel inverter or series H-bridge

inverter. The series H-bridge inverter appeared in 1975. Cascaded multilevel inverter was not fully realized until two researchers, Lai and Peng. They patented it and presented its various advantages in 1997. Since then, the CMI has been utilized in a wide range of applications. With its modularity and flexibility, the CMI shows superiority in high-power applications, especially shunt and series connected FACTS controllers. The CMI synthesizes its output nearly sinusoidal voltage waveforms by combining many isolated voltage levels. By adding more H-bridge converters, the amount of Var can simply increased without redesign the power stage, and build-in redundancy against individual H-bridge converter failure can be realized. A series of single-phase full bridges makes up a phase for the inverter. A three-phase CMI topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters, which can possibly generate different output voltage waveforms and offers the potential for AC system phase-balancing. This feature is impossible in other VSC topologies utilizing a common DC link. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link supply for each full bridge converter is provided separately, and this is typically achieved using diode rectifiers fed from isolated secondary windings of a three-phase transformer. Phase-shifted transformers can supply the cells in medium-voltage systems in order to provide high power quality at the utility connection.

VI. Seven level cmi

The converter topology is based on the series connection of single-phase inverters with separate dc sources. Fig. 2.11 shows the power circuit for one phase leg of a three-level, five-level and seven-level cascaded inverter. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: $+V_{dc}$, 0, $-V_{dc}$ (zero, positive dc voltage, and negative dc voltage). This is made possible by connecting the capacitors sequentially to the ac side via the power switches. The resulting output ac voltage swings from $-V_{dc}$ to $+V_{dc}$ with three levels, $-2V_{dc}$ to $+2V_{dc}$ with five-level and $-3V_{dc}$ to $+3V_{dc}$ with seven-level inverter. The staircase waveform is nearly sinusoidal, even without filtering.

For a three-phase system, the output voltage of the three cascaded converters can be connected in either wye (Y) or delta (Δ) configurations. For example, a wye-configured 7-level converter using a CMC with separated capacitors is illustrated in the fig

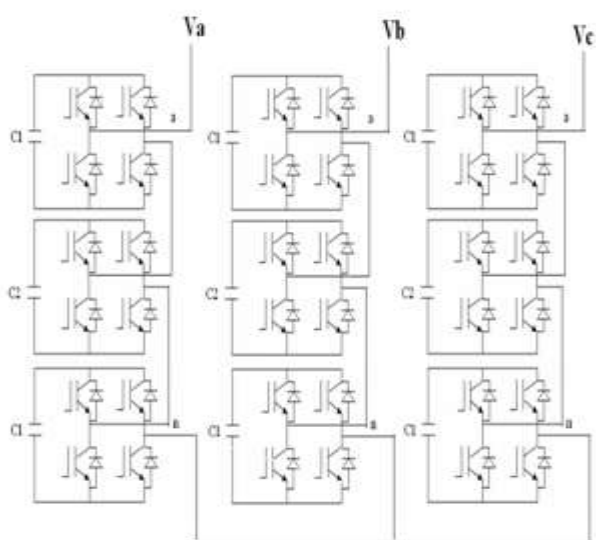


Fig.7.Three-phase 7-level cascaded multilevel inverter (Y-configuration)

VII. Features of CMLI

For real power conversions, (ac to dc and dc to ac), the cascaded-inverter needs separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic, and biomass, etc.

Connecting separated dc sources between two converters in a back-to-back fashion is not possible because a short circuit will be introduced when two back-to-back converters are not switching synchronously.

In summary, advantages and disadvantages of the cascaded inverter based multilevel voltage source converter can be listed below.

VIII. Advantages

- i) The regulation of the DC buses is simple.
- ii) Modularity of control can be achieved. Unlike the diode clamped and capacitor clamped inverter where the individual phase legs must be modulated by a central controller, the full-bridge inverters of a cascaded structure can be modulated separately.
- iii) Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.
- iv) Soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers.

Disadvantages

- i) Communication between the full-bridges is required to achieve the synchronization of reference and the carrier waveforms.

- ii) Needs separate dc sources for real power conversions, and thus its applications are somewhat limited

IX. Symmetrical Cascaded H-Bridge multilevel Inverter

If all the input sources are of equal magnitude, it is known as Symmetrical H-Bridge inverter as shown. The switching sequence is given in table 3. Here both the full bridge inverters are fed with different sources of equal magnitude.

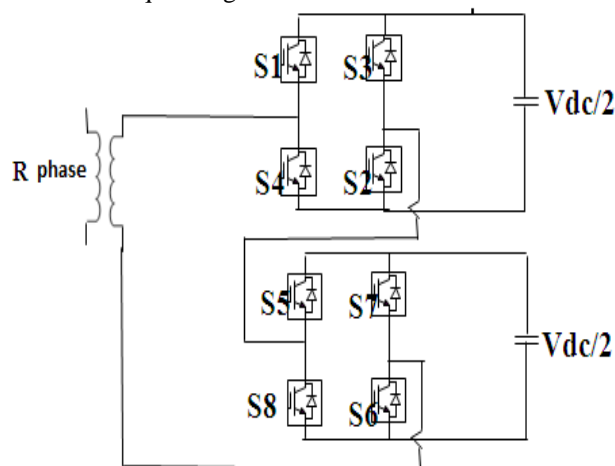


Fig.8.Symmetrical five level Cascaded H-Bridge inverter

In the above fig, each SDCS of equal magnitude is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. By different combinations of the four switches, S1-S4, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$, and zero. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. In this topology, the number of output phase voltage levels is defined by $m = 2s + 1$, where s is the number of dc sources.

A 5-level cascaded-inverters will have two SDCSs and two full-bridge cells. The switching table for the five level cascaded inverter is shown below. Here, 2 Full Bridges are used and are cascaded to each other. The Switches S1, S2, S3, and S4 are from upper H-Bridge and Switches S5, S6, S7 and S8 are from lower H-Bridge. By giving correct switching pattern, we get 5 voltage levels i.e $2V_{dc}, V_{dc}, 0, -2V_{dc}, -V_{dc}$. To get $2V_{dc}$, S1,S2,S5,S7 are on. To get V_{dc} , S1,S2,S6,S5 are kept on. The switching table is shown below to get 5 levels with a Symmetrical DC source.

Table: Switching states of Symmetrical five level cascaded H-Bridge inverter

Switches ON	Voltage level
S1, S2, S5 and D7	$V_{dc}/2$
S1, S2, S6 and S5	V_{dc}
S1, S2, S6 and D8	$V_{dc}/2$
S1, D3, S6 and D8	0
S3, S4, S6 and D8	$-V_{dc}/2$
S3, S4, S7 and S8	$-V_{dc}$
S3, S4, D6 and S8	$-V_{dc}/2$
S1, S3, D6 and S8	0

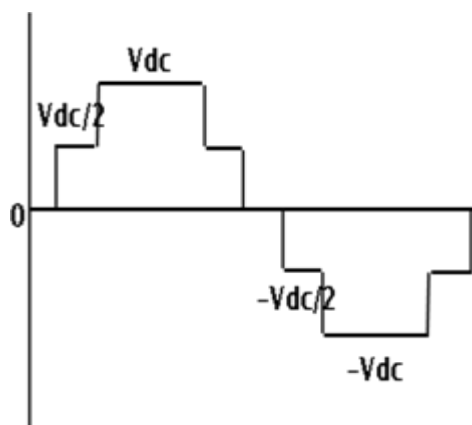


Fig.9. Output waveform of Symmetrical Cascaded H-Bridge multilevel Inverter

X. Asymmetrical Cascaded H-Bridge multilevel Inverter

The cascaded H-Bridge multi level inverter with two SDCS with unequal magnitude is known as Asymmetrical Cascaded H-Bridge multilevel Inverter. The following is figure 2.15 of Asymmetrical Cascaded H-Bridge multilevel Inverter where it is having 2 unequal DC sources $+2V_{dc}/3$ and $+V_{dc}/3$.

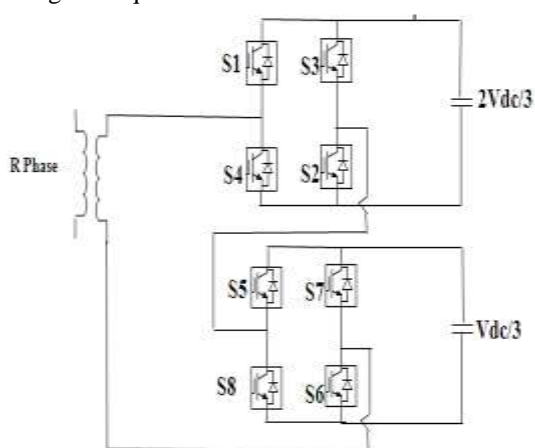


Fig.10. Asymmetrical Cascaded H-Bridge multilevel Inverter

By using this type of Asymmetrical configuration, for a 'n' bridge inverter we can get $3n+1$ voltage levels and n Capacitors of each rating $nV_{dc}/(n+1)$, $V_{dc}/(n+1)$ to get V_{dc} max and $6n$ switches of each voltage rating is $V_{dc}/(n+1)$. The following is the switching table of Asymmetrical Cascaded H-Bridge multilevel Inverter.

Table: Switching states of Asymmetrical five level cascaded H-Bridge inverter

Switches ON	Voltage level
S4, S2, S5 and S6	$V_{dc}/3$
S1, S2, S8 and S6	$2V_{dc}/3$
S1, S2, S5 and S6	V_{dc}
S4, S2, S7 and S8	$-V_{dc}/3$
S3, S4, S6 and S8	$-2V_{dc}/3$
S3, S4, S7 and S8	$-V_{dc}$
S4, S2, S8 and S6	0

Simulink model:

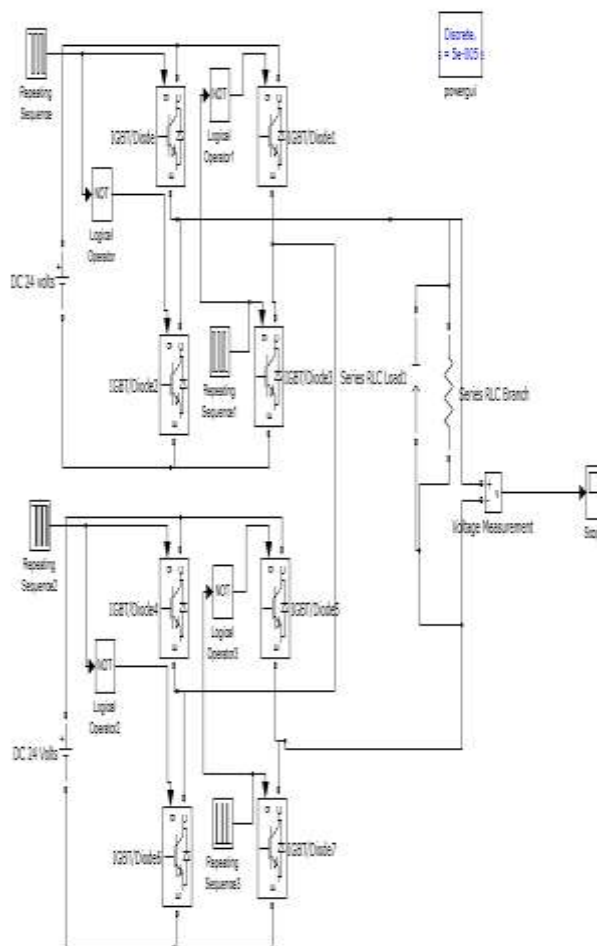


Fig.10. Simulink model

XI. Matlab/simulation results
comparitive simulink results for three ,five ,seven level inverters:

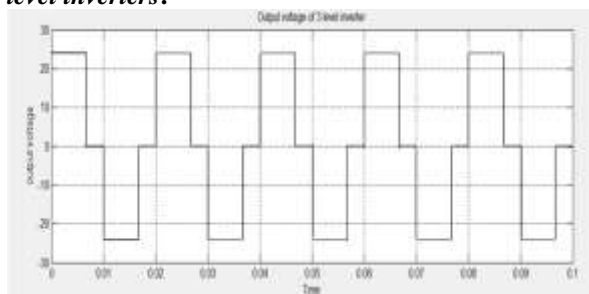


Fig.11. Simulink results for three level inverter

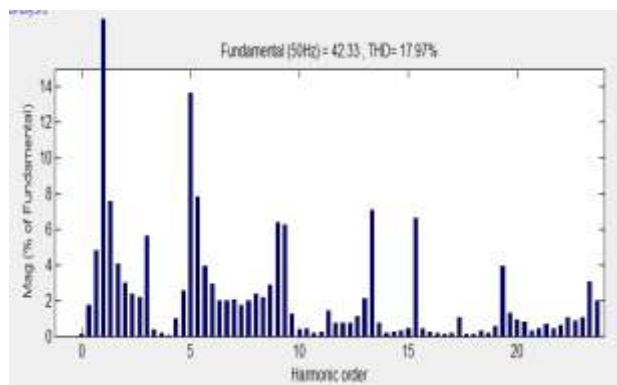


Fig.16. Analysis for seven level inverter

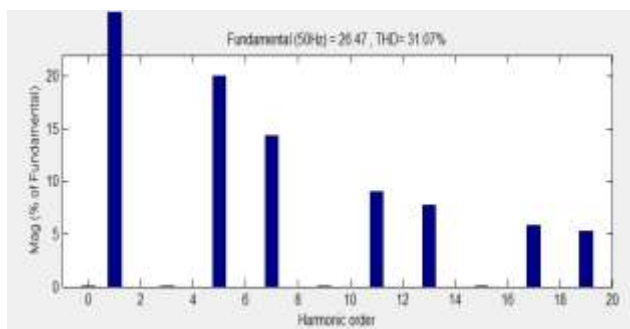


Fig.12. Analysis for three level

Simulink results for different levels of symmetrical inverters:

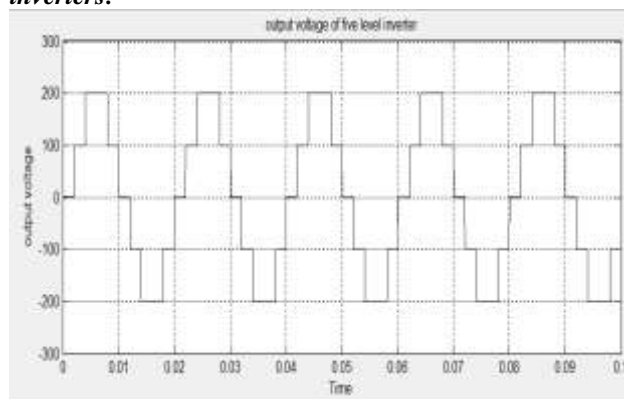


Fig.17. Output waveform of five level inverter

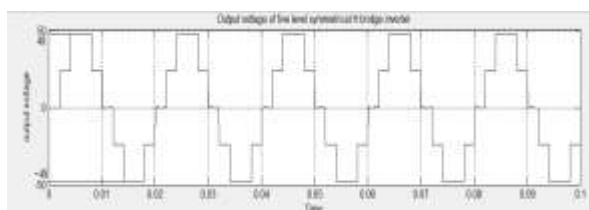


Fig.13. Simulink results for a practical voltage of 48 volts for five level inverter

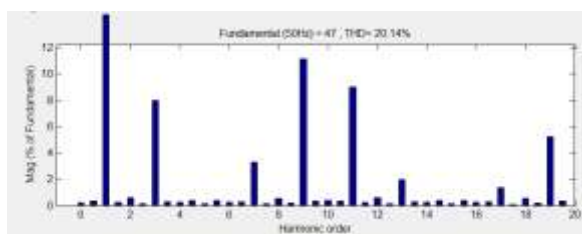


Fig.14. THD analysis for five level inverter

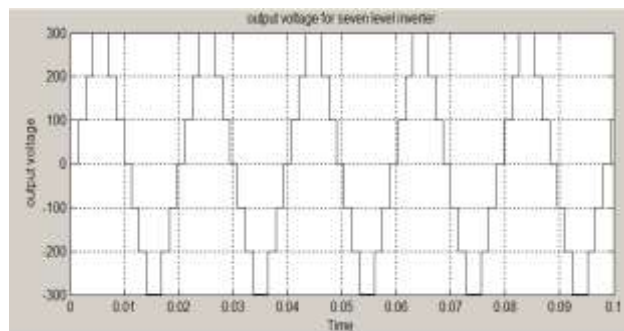


Fig.18. The output waveform for seven level inverter

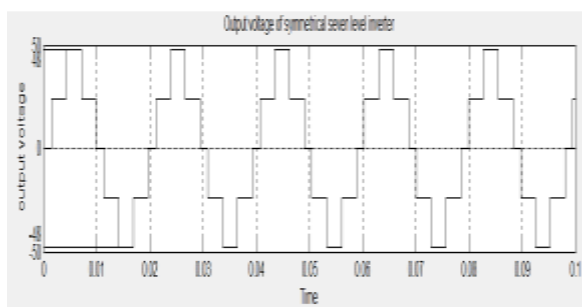


Fig.15. Simulink results for a seven level inverter

Hard ware implementation:

Microcontroller:

Microprocessors and microcontrollers are widely used in embedded systems products. Microcontroller is a programmable device. A microcontroller has a CPU in addition to a fixed amount of RAM, ROM, I/O ports and a timer embedded all on a single chip. The fixed amount of on-chip ROM, RAM and number of I/O ports in microcontrollers makes them ideal for many applications in which cost and space are critical.

The Intel 8052 is Harvard architecture, single chip microcontroller (μ C) which was developed by Intel in 1980 for use in embedded systems. It was

popular in the 1980s and early 1990s, but today it has largely been superseded by a vast range of enhanced devices with 8052-compatible processor cores that are manufactured by more than 20 independent manufacturers including Atmel, Infineon Technologies and Maxim Integrated Products.

8052 is an 8-bit processor, meaning that the CPU can work on only 8 bits of data at a time. Data larger than 8 bits has to be broken into 8-bit pieces to be processed by the CPU. 8052 is available in different memory types such as UV-EPROM, Flash and NV-RAM.

The present project is implemented on KeilUvision. In order to program the device, proload tool has been used to burn the program onto the microcontroller.

The features, pin description of the microcontroller and the software tools used are discussed in the following sections.

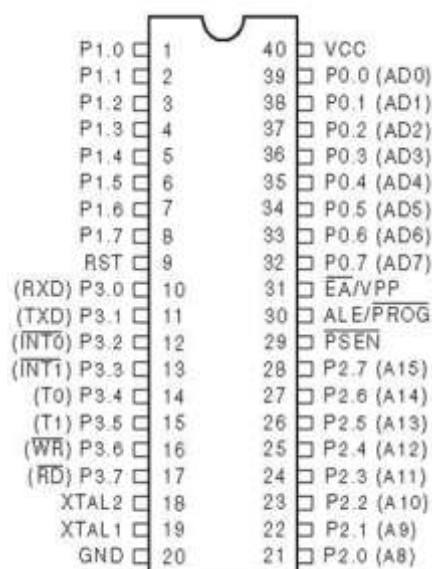


Fig.19. Pin diagram

Features of AT89s52:

1. 4K Bytes of Re-programmable Flash Memory.
2. RAM is 128 bytes.
3. 2.7V to 6V Operating Range.
4. Fully Static Operation: 0 Hz to 24 MHz
5. Two-level Program Memory Lock.
6. 128 x 8-bit Internal RAM.
7. 32 Programmable I/O Lines.
8. Two 16-bit Timer/Counters.
9. Six Interrupt Sources.
10. Programmable Serial UART Channel.
11. Low-power Idle and Power-down Modes.

XII. Description

The AT89S52 is a low-voltage, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcomputer, which provides a highly flexible and cost-effective solution to many embedded control applications.

In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

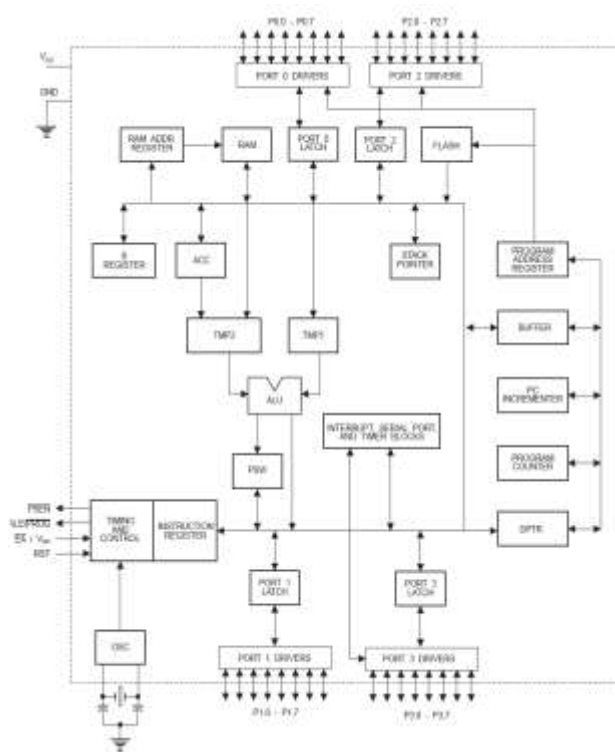


Fig.20. Block diagram

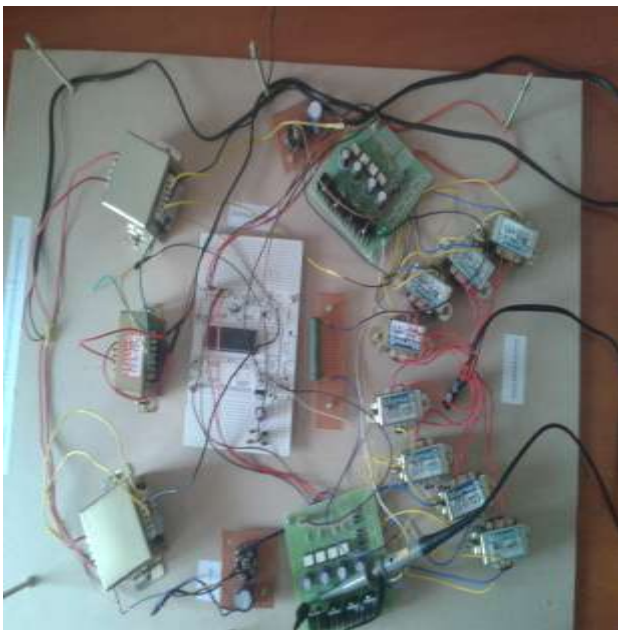


Fig.21.Hardware kit

XIII. Hardware results

The proposed inverter is constructed in hardware.

The input for the DC bus for upper H bridge is given by 230/24V transformer through a diode bridge followed by capacitive filter. The DC voltage obtained is around 40V. The input for the lower H bridge is given by 230/12V transformer through a diode bridge followed by capacitive filter. The DC voltage obtained is around 20V. The voltage steps in the outputs are therefore 0V, 20V, 40V, 60V, -20V, -40V and -60V. The voltage output obtained is as follows.

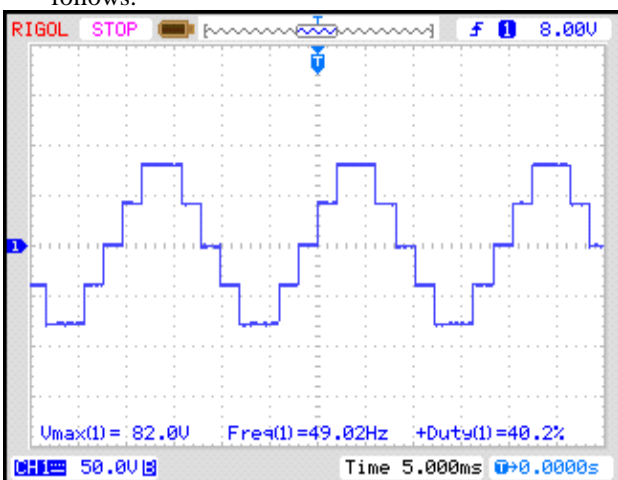


Fig.22. output of the inverter.

The gating pulses are generated by AT89S52 micro controller.

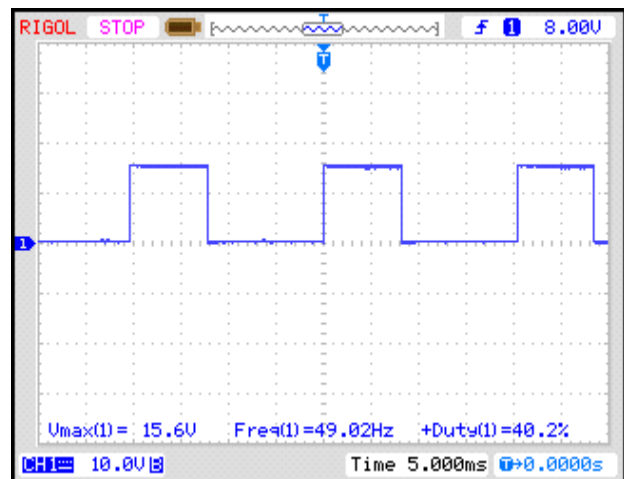


Fig.23. Gating pulse of switch1

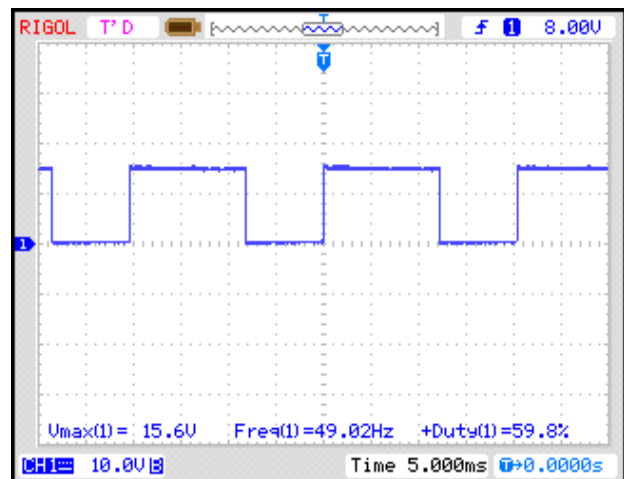


Fig.24. Gating pulse of switch2

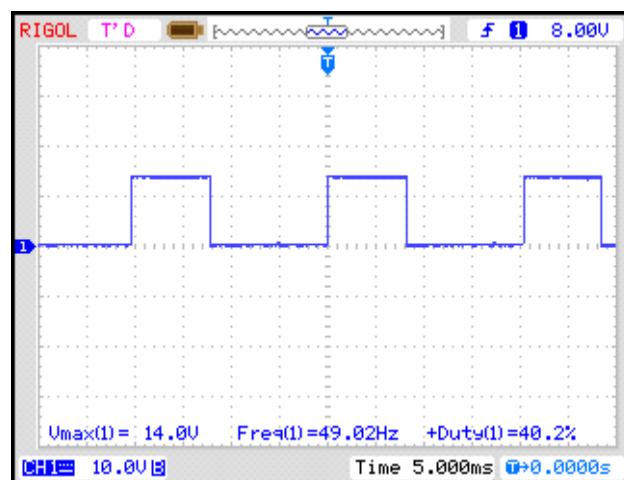


Fig.25. Gating pulse of switch3

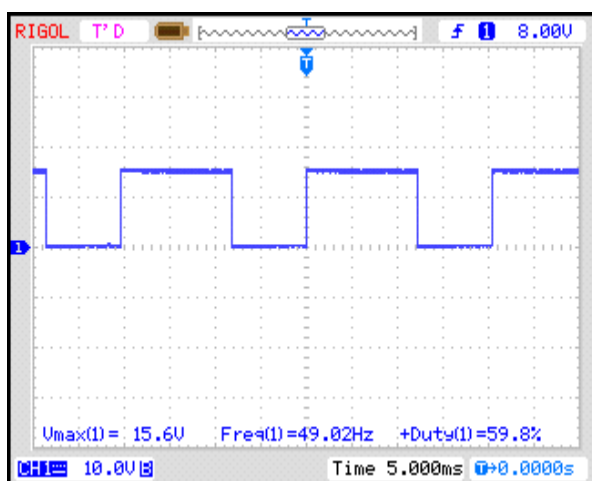


Fig.26.Gating pulse of switch4

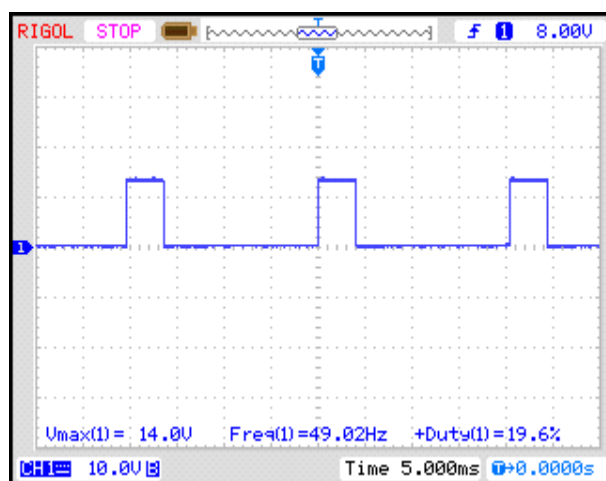


Fig.29.Gating pulse of switch7

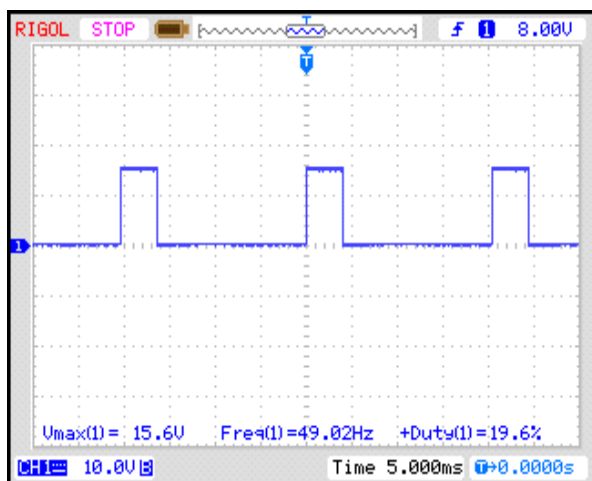


Fig.27.Gating pulse of switch5

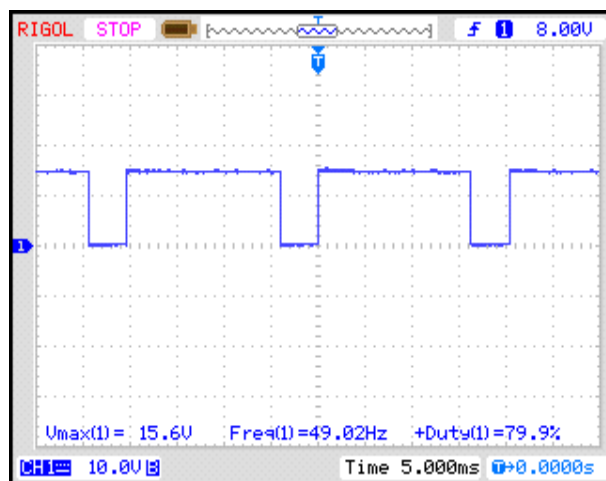


Fig.30.Gating pulse of switch8

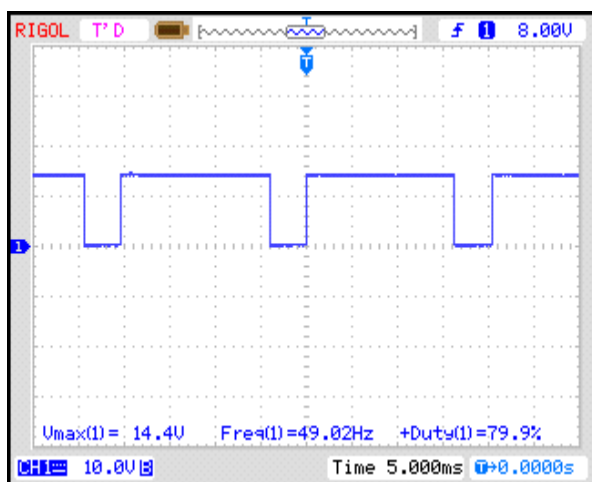


Fig.28.Gating pulse of switch6

Comparison of power component requirements per phase leg among different multilevel Inverters

Inverter Configuration	Diode clamped	Flying capacitor	Cascaded H-Bridge
Main switching Devices	$2(m-1)$	$2(m-1)$	$2(m-1)$
Main Diodes	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping Diodes	$(m-1)(m-2)$	0	0
DC bus Capacitors	$m-1$	$m-1$	$(m-1)/2$
Balancing Capacitors	0	$(m-1)(m-2)/2$	0

XIV. Advantages

1. The regulation of the DC buses is simple.
2. Modularity of control can be achieved. Unlike the diode clamped and capacitor clamped inverter where the individual phase legs must be

- modulated by a central controller, the full-bridge inverters of a cascaded structure can be modulated separately.
3. Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.
 4. Soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers.
 5. Conclusion :
 6. CHB multilevel inverter has low stress, high conversion efficiency and can also be easily interfaced with renewable energy sources (PV, Fuel cell etc.).
 7. Asymmetrical CHB multilevel inverter uses least number of devices to produce higher voltage level.
 8. As number of level increases, the THD content approaches to small value as expected. Thus it eliminates the need for filter.
 9. Though, THD decreases with increase in number of levels, some lower or higher harmonic contents remain dominant in each level. These will be more dangerous in Induction drives.
 10. Hence the future work may be focused on implementing closed loop control with suitable harmonic elimination technique to achieve better performance of the converter.

REFERENCES

- [1] N. Ravisankar Reddy, T. Brahmananda Reddy, I. Amamath, and D. SubbaRayudu, "Hybrid PWM Algorithm for Vector Controlled Induction Motor Drive without Angle Estimation for Reduced Current Ripple", ICGST-ACSE journal, ISSN: 1687-4811, Volume 9, Issue 3, December 2009.
- [2] S.Albert Alexander, T. Manigandan, N. Senthilnathan, "Digital Switching Scheme for Cascaded Multilevel Inverters" Third International Conference on Power Systems, Kharagpur, INDIA December 27-29,2009.
- [3] Leon M Tolbert and Thomas G Habetler, "Novel Multilevel inverter Carrier based PWM method", IEEE Transactions on Industry Applications vol. 35, no.5, pp. 1098-1107, September/ October 1999.
- [4] C. Govindaraju and Dr.K. Baskaran, "Optimized Hybrid Phase Disposition PWM Control Method for Multilevel Inverter" International Journal of Recent Trends in Engineering, Vol I, No. 3, May 2009.
- [5] B.Diong and K.Corzine, "WTHD optimal staircase modulation of single-phase multilevel inverter" Texas Christain University, USA.
- [6] Keith A. Corzine, Mike W. Wielebski, Fang Z. Peng, and Jin Wang, "Control of Cascaded Multilevel Inverters" on power electronics May 2004.
- [7] L.M.Tolbert, F.z.Peng and T.G. Habetler, "Multilevel converters for Large Electric Drives," IEEE Transactions on Industry Applications, vol. 35, no.5, pp.36-44, January | February 1999.
- [8] Jose Rodriguez, Steffen Bernet and Bin Wu, "Multilevel voltage source converter topologies for Industrial medium voltage Drives," IEEE Transactions on Industrial Electronics, vol.54, no.6, pp.2930-2945, December 2007.
- [9] F.Huang, "Near optimal approach in the design and implementation of multilevel voltage source inverter", IEE -Proc -Electr Power Appl., VoI 146, No 6, pp. 661-666, November 1999. 300
- [10] Q.Jiang and T.A Lipo, "Switching angles and DC link voltage optimization for multilevel cascaded inverters", Electric machines and Power Systems, V 28, n 7, p 605-612, July 2000.
- [11] Yu Liu, Hoon Hong, and Alex Q. Huang, "Real Time algorithm for minimizing THD in multilevel inverters using unequal or varying voltage steps under stair case modulation", IEEE Transactions on Industrial Electronics, vol. 56, no.6, pp. 2249-2258, June 2009.
- [12] Yu Liu, Hoon Hong, and Alex Q. Huang, "Real time calculation of switching angles minimizing THD for multilevel inverters with step modulation", IEEE Transactions on Industrial Electronics, vol. 56, no.6, pp. 285-293, February 2009.